blocks [E] and/or [F], wherein S1, S2,...Sn are serial input bit lines of said architecture [A], n representing a number of coefficients of the filter transfer function;

wherein said architecture [A] includes m combinational logic blocks [B] consisting of full adder and full subtractor elements and the blocks [B] provide the addition terms of the filter transfer function [(a0*S1+b0*S2+...+k)*Sn), (A1*S1+b1*S2+...+k1*Sn)...(am*S1+bm*S2+...+km*Sn)], where a0, b0...k0, a1, b1...k1, am, bm, ...km are (+/-1 or 0);

wherein the connection of the FA and/or FS elements to the S1, S2... Sn lines and interconnection of the Fa and FS elements depend on the value of coefficients a0...km;

wherein the final output of a last FA or FS element of each block [B] is terminated through lines b_1, b_2...b_m at a plurality of delay elements [T] within a logic block [C], the number of delay elements [T] depending on the size of a maximum coefficient value of the filter transfer function and being shareable by blocks [B];

wherein in said architecture [A] the blocks [B] are clustered together in series to form block [D] and delay elements [T] are clustered together in block [C], thereby spatially separating the sequential and combinational logic blocks;

wherein in said architecture [A], the output of each delay element [T] is connected to one of the inputs of one of the FA or FS elements of a respective block [B] corresponding to a next bit position;

wherein the interconnections between blocks [C] and [B] are represented as t_1, t_2, ...t_m, the FA and/or FS elements are arranged in matrix form such that elements FA0_0 to FA0_n correspond to bit position 0, elements FA1_1 to FA1_n correspond to bit position 1, and elements FAm_1 to FAm_n correspond to bit position m;

wherein the carry-out pin of each FA or FS element of each block [B] is fed to the input of an FA or FS element of a previous block [B] such that the same delay element [T] is used for multiplication by a factor of two and also for the carry structure in a one bit serial adder function;

wherein in the said architecture [A] logic components represented as block [Ex] are used for connecting the carryout of the FA and FS elements in a last stage of block [D] and a plurality of FA and/or FS elements and delay elements [T] are used within one block [Ex];

whereby said architecture [A] is structured into sequential block [C] consisting of delay elements and combinational block [D] consisting of FA and/or FS elements, while the delay elements [T] of block [C] are each position at a respective end position of each block [B], block [D] includes combinational element blocks [B] which essentially include FA and/or FS elements, thereby forming shareable logic elements within block [D]; and

a final output of the architecture [A] is a bit in the m^{th} position.

2. The device as claimed in claim 1 wherein when operated in bit serial fashion, the device provides hardware minimization of a finite impulse response filter, an infinite impulse response filter or for other filters, and application related to combinational logic consisting of delay elements [T], multiplier elements [M], and FA and/or FS elements.

3. The device as claimed in claim 1 wherein block [D] uses an FS element instead of an FA element when a filter transfer function coefficient value is close to a power of two.

4. The device as claimed in claim 1 wherein block [D] minimizes the use of FS elements by using a common subtraction operator and substituting FA elements instead.

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5. (Amended) The device as claimed in claim 1 wherein coefficient lines CLin_0... Clin_n are not derived from a common input line but are instead respectively delayed by 0...n unit delays prior to input into said architecture [A].

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6. (Amended) The device as claimed in claim 1 wherein instead of FA and FS elements, sequential adder and sequential subtractor elements are used.

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7. A bit serial FIR filter device including:

a logic block [A] adapted to receive an (m+1)-bit input and to produce a transfer function output corresponding to the m^{th} bit position, block [A] including:

a combinational-sequential logic block [D] adapted to receive a filter transfer function coefficients S1, S2, ...Sn or a predetermined transfer function and including m+1 combinational logic blocks B0, B1, ...Bm; and

a sequential logic block [C] having m delay elements T1, T2, ...Tm for receiving respective outputs of blocks B0, B1, ...Bm-1 and for providing delayed outputs to respective blocks B1, B2, ...Bm;

wherein each block Bx, for x=0,1...m, includes a plurality of serial subtractor or adder elements [SA], up to a maximum of n, SAx_1, SAx_2...SAx_n, for providing a coefficient multiplication function for each block Bx; and

wherein block Bm outputs said transfer function output according to said transfer function, based on said (m+1)-bit input.

Please add new claims 8-17 to read as follows:

8. (New) A digital filter device comprising:

a coefficient circuit having *n* input bits corresponding to *n* filter coefficients;

a combinational circuit comprising a plurality of full adders with the interconnection of the plurality of full adders depending on values of the *n* coefficients to implement the addition terms of the filter transfer function; and

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a sequential circuit comprising a predetermined number of unit delays with the predetermined number being dependent on a maximum value of the *n* coefficients, the inputs of the unit delays being coupled to output of selected ones of the full adders and the output of the unit delays being coupled to an input of a full adder in an adjacent bit position from the corresponding unit delay.

9. (New) The filter of claim 8 wherein the combinational circuit implements the addition terms of the filter transfer function using the following form:

(a0*S1+b0*S2+...+k)*Sn),

(a1*S1+b1*S2+...+k1*Sn),

...

(am*S1+bm*S2+...+km*Sn)],

where S1, S1, Sn are filter coefficients and

a0, b0...k0, a1, b1...k1, am, bm, ...km are (+/-1 or 0).

10. (New) The filter of claim 8 wherein the coefficient circuit receives *n* serial input bits.

11. (New) The filter of claim 8 wherein the combinational circuit and the sequential circuit are interconnected to implement a finite input response (FIR) filter.

12. (New) The filter of claim 8 wherein the combinational circuit and the sequential circuit are interconnected to implement an infinite input response (IIR) filter.

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13. (New) A method of implementing a digital filter comprising:

generating *n* filter coefficients using a combinational logic circuit comprising a plurality of full adders with the interconnection of the plurality of full adders depending on values of the *n* coefficients to implement addition terms of the filter transfer function; and

generating a plurality of multiplication factors sequential logic circuit comprising a predetermined number of unit delays with the predetermined number being dependent on a maximum value of the *n* coefficients, the inputs of the unit delays being coupled to output of selected ones of the full adders and the output of the unit delays being coupled to an input of a full adder in an adjacent bit position from the corresponding unit delay.

14. (New) The method of claim 13 wherein the digital filter has *n* serial input bits corresponding to *n* filter coefficients.

15. (New) The method of claim 14 wherein the *n* input bits are serial input bits.

16. (New) The method of claim 13 wherein the combinational circuit and the sequential circuit are interconnected to implement a finite input response (FIR) filter.